**Design of a 32 - bit core based on RISC – V Architecture**

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**Introduction**

RISC – V is an open-source RISC processor specification. It was developed at UC, Berkeley. It is the fifth iteration in a series of RISC architectural designs done by UC Berkeley. In this project, 32 – bit Core based on the RISC – V ISA is designed.

**Motivation**

x86-based instructions (CISC) are difficult to decode and hence slower to execute. Moreover, since the x86 architecture has very less number of processor registers, most of instructions are executed in the memory or cache, causing more power consumption. The RISC – V Architecture has an advantage here with **31** general-purpose registers. All the instructions are of fixed width (32 – bit).

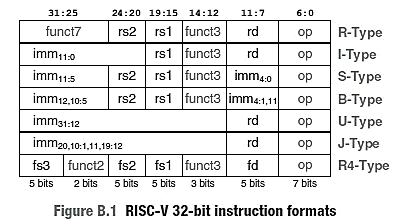
RISC – V is potentially suitable for various applications ranging from micro-power embedded devices to high-performance server-based cloud multiprocessors. Most importantly, RISC – V is an **open-source** ISA unlike most other architectures.

**Languages, Tools and Technologies used**

Verilog, System Verilog, Intel Quartus Prime Lite, ModelSim - Altera

**Instruction Set of the processor**

Our processor aims to support the **RV32I** Core instructions.



**Figure 1**: **RV32I** Instruction types and their formats

**Instruction Execution Cycle**

It has **five** stages: Fetch, Decode, Execute, Memory Access and Write back

**Design Details**

32 – bit processor with 5 stage **pipelined** microarchitecture based on RISC - V. It executes an instruction in five stages.

It also has a **Hazard Unit** to handle both Data Hazards and Control Hazards

System Verilog is used for behavioural modelling of the processor.

Intel Quartus Prime Lite will be used as the platform for generating gate – level netlist, and for visualizing the output waveform.

**Performance Analysis**

**CPI (Cycles per Instruction) = 1,** for Single Cycle Processor. The clock speed in a single-cycle processor is limited by the slowest instruction.

**References**

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